REMARKS/ARGUMENTS

Applicants representative would like to thank Examiner Vartanian for taking the time to conduct a telephonic interview to discuss the remaining issues in this case. As noted in the interview summary, the claims were discussed in light of U.S. Patent No. 4,584,695 to *Wong et al*, and U.S. Patent No. 4,975,634 to *Shohet*, but an agreement was not reached on the allowability of the claims over *Shohet*.

Further comparison of *Shohet* with the pending claims reveals that the reference neither teaches nor suggests all the elements of the claims. Accordingly, reconsideration and withdrawal of the rejection of claims 1–2, 5, 7–11, and 16 under 35 U.S.C. § 102(b), and claims 6, 15, 17, and 19–23 under § 35 U.S.C. § 103(a) over *Shohet* is respectfully requested in light of the following remarks.

Claim 1 includes a method of measuring jitter in a digital signal where an offset reference clock signal is formed that is "offset by a predetermined frequency amount from said digital signal." *See* claim 1, lines 2–3. Similarly, claims 10 and 15 include a means and an offset unit, respectively, which form an offset reference clock signal that is offset by a predetermined frequency amount from the digital signal. *See* claims 10 and 15, lines 3–4. As the specification notes, "[t]he effect of the offset of the reference clock signal is that the sampling point is not fixed relative to the transition point over the bits of the input signal, but instead moves relative thereto." *See* Specification, page 2, line 26 to page 3, line 3. The present invention takes advantage of the relative motion of the offset reference clock signal and the input (*i.e.*, digital) signal to scan the pulses in the pulse-train of the digital signal. *See, e.g.,* Specification, page 10, lines 8–25.

In contrast, *Shohet* does just the opposite by making sure the reference clock signal and digital signal are frequency synchronized during a jitter measurement. The jitter measurement device in *Shohet* includes a range adjusting circuit that includes gang switches to insure any adjustment in clock signal frequency is matched in the jittered clock (*i.e.*, digital) signal frequency:

> A range adjusting circuit 20, to be explained more fully below, adjusts the frequency of the high frequency clock signal f_{Ho} from terminal 14 and the jittered clock signal f_{Jo} from terminal 16. The adjustment is illustrated as a pair of gang switches such that the adjustment of the high frequency clock f_H and the jittered clock signal f_{Jo} are both adjusted by the similar amount to produce signals f_H and f_J.
>
> *Shohet*, Col. 2, lines 57–64.

Shohet does describe the ability to adjust the relative *phase* of the two clock signals, but a phase adjustment is not the same thing as a frequency offset. *Shohet*, Col. 3, lines 50–56. Adjusting the *phase* of the reference clock signal relative to the jittered clock signal does not change the *frequency* of either signal. After a phase adjustment, the reference clock and jittered clock signals remain fixed with respect to each other (except for jitter) during the jitter measurement. There is no description or suggestion in *Shohet* that frequencies be adjusted (*i.e.*, offset) so that the reference clock signal moves over the jittered clock signal during a jitter measurement. If anything, *Shohet* teaches away from having the reference signal moving relative to the jittered clock signal during the measurement, because this movement would be read as a jitter measurement by the measurement device. *Shohet* Col. 3, lines 31–34.

Shohet neither describes nor suggests all the elements of claims 1, 10, and 15, and these claims are allowable over the reference. For at least the same reason, claims 2–3, 5–9, 11–12, and 16–23, which depend from claims 1, 10 and 15, respectively, are also allowable over *Shohet*. Accordingly, withdrawal of the rejection of claims 1–2, 5, 7–11, and 16 under 35 U.S.C. § 102(b), and claims 6, 15, 17, and 19–23 under § 35 U.S.C. § 103(a) over *Shohet* is respectfully requested.

CONCLUSION

Formal drawings have been provided with this Response that correct the informalities in Figs. 4–7. In view of the submission of formal drawings and the remarks above, Applicants believe pending claims 1–3, 5–12, and 15–23, are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 303-571-4000.

Respectfully submitted,

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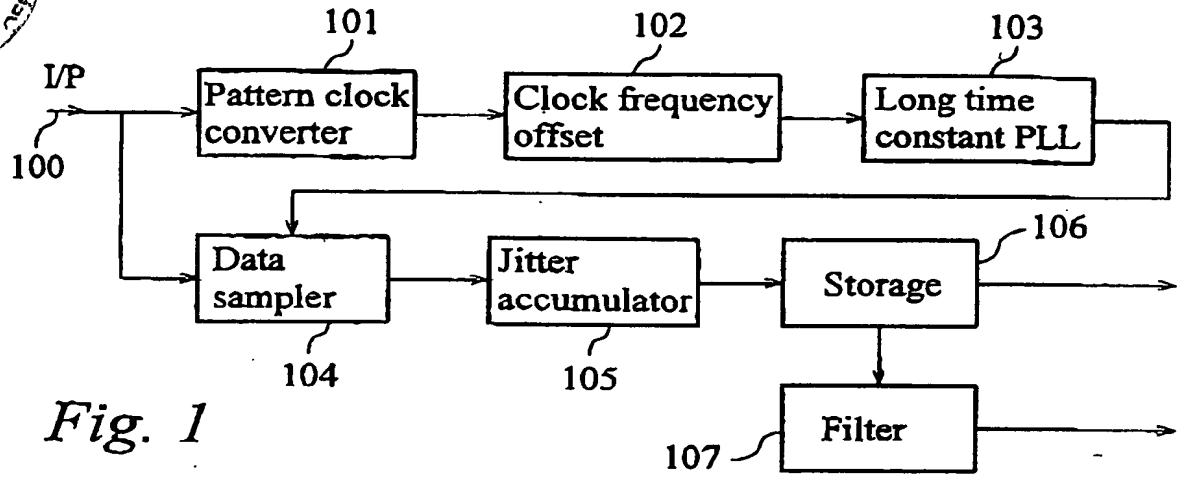
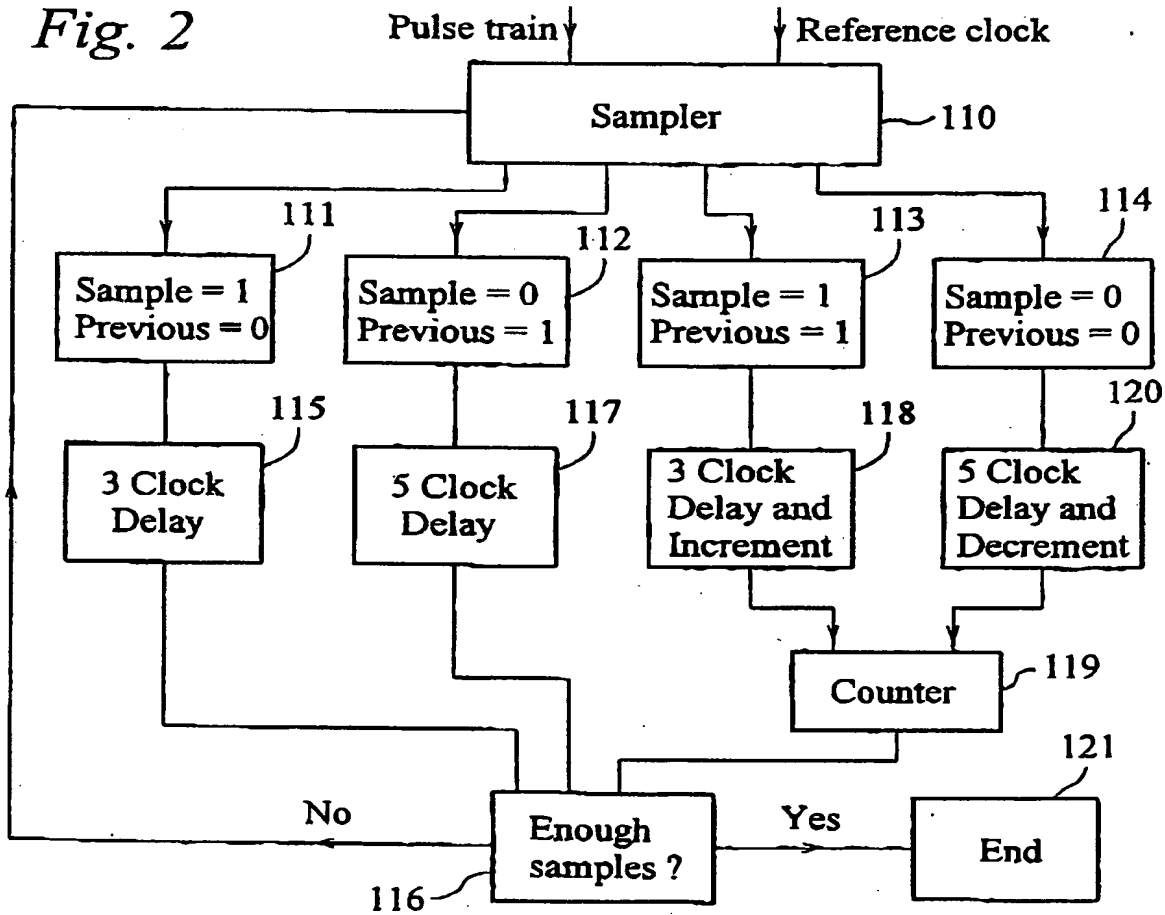


Fig. 1

Fig. 2



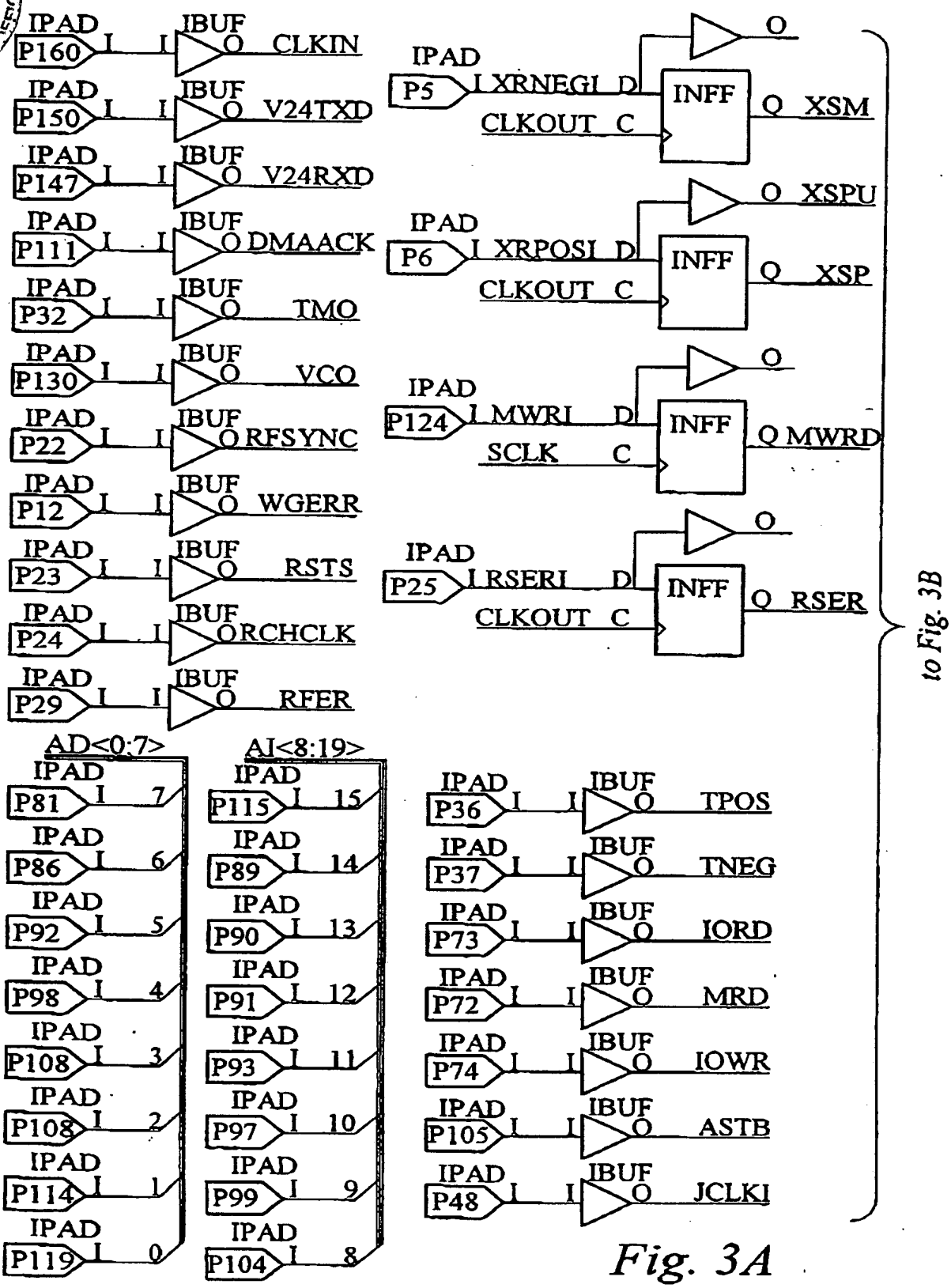


Fig. 3A

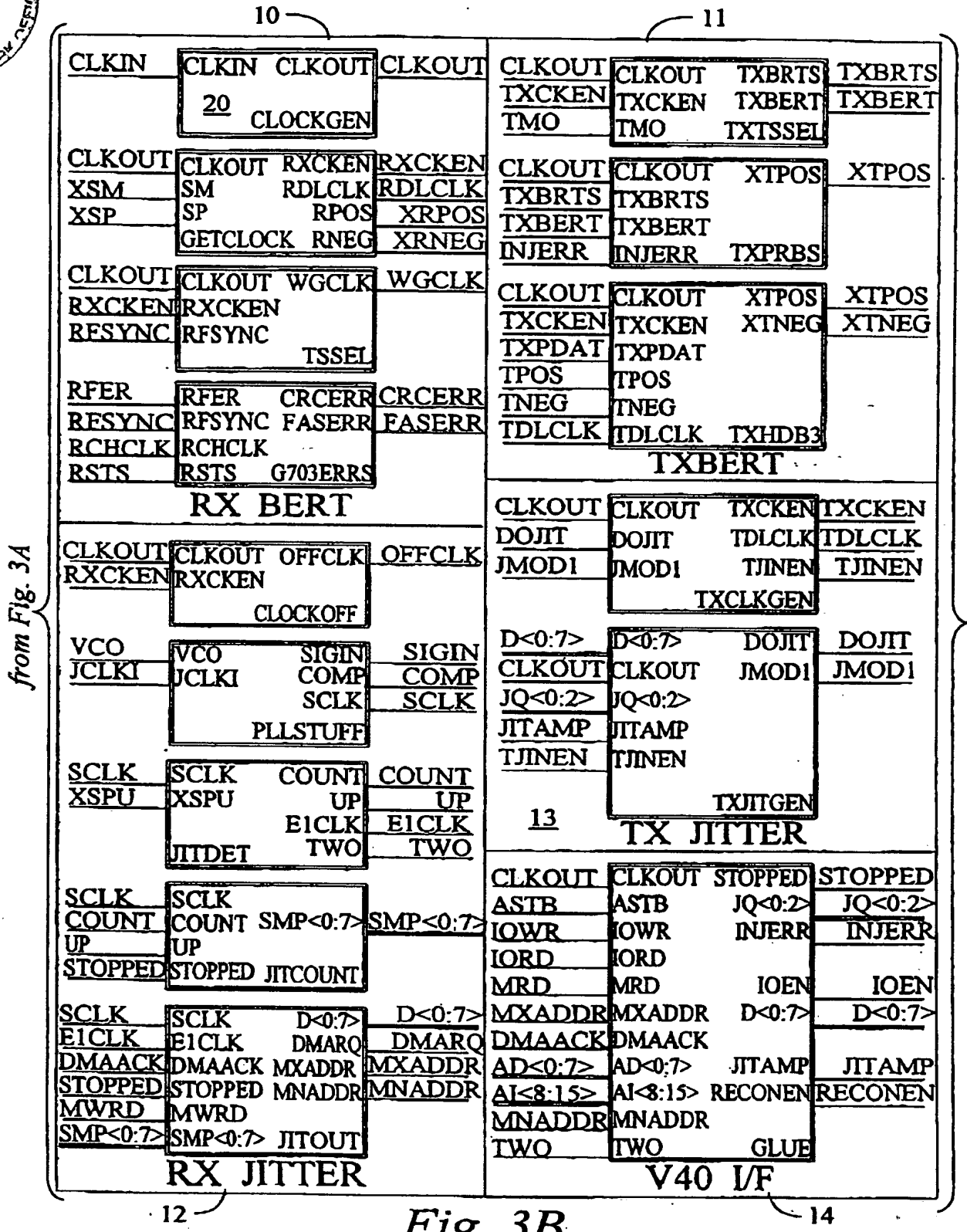


Fig. 3B

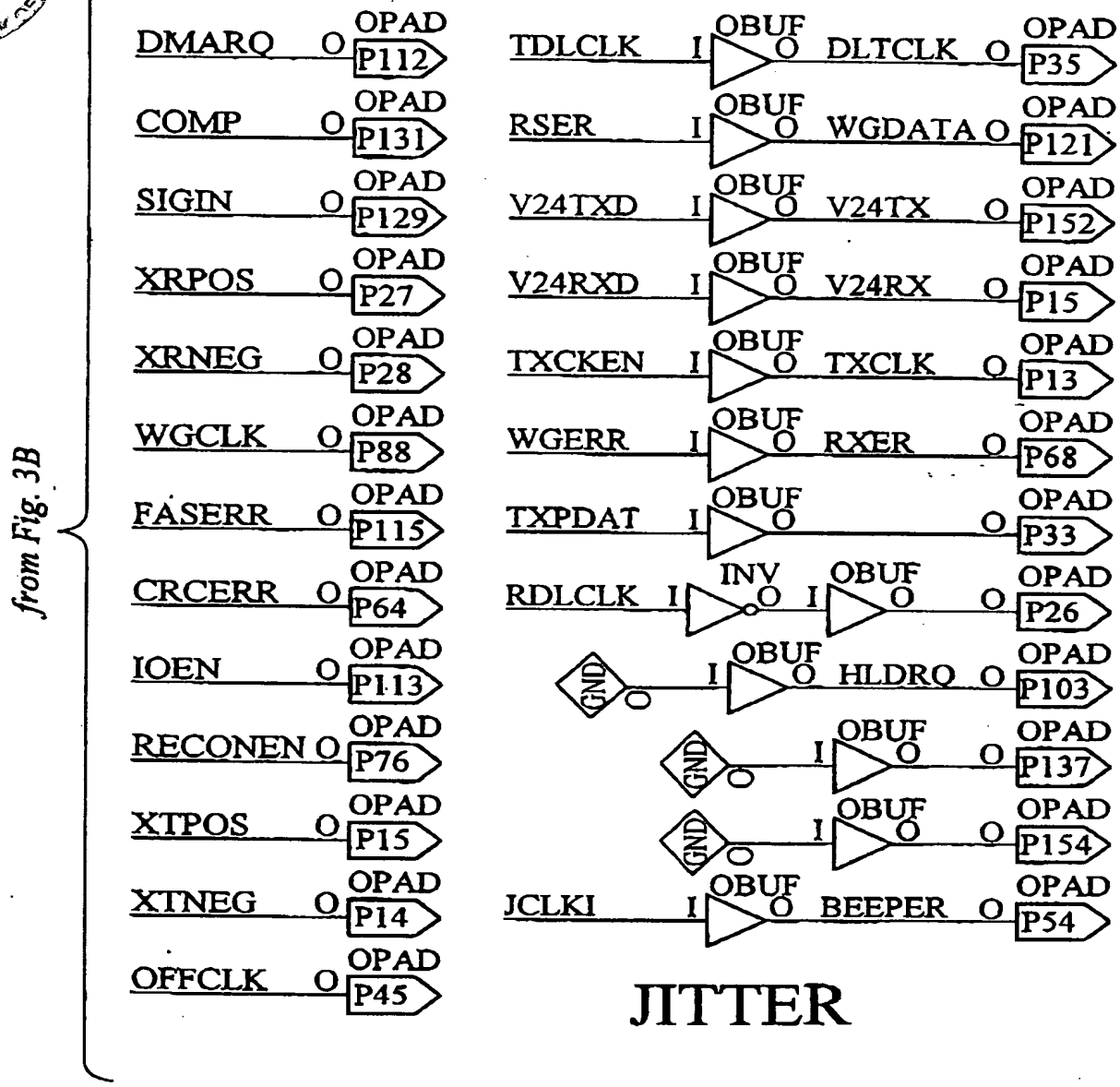


Fig. 3C

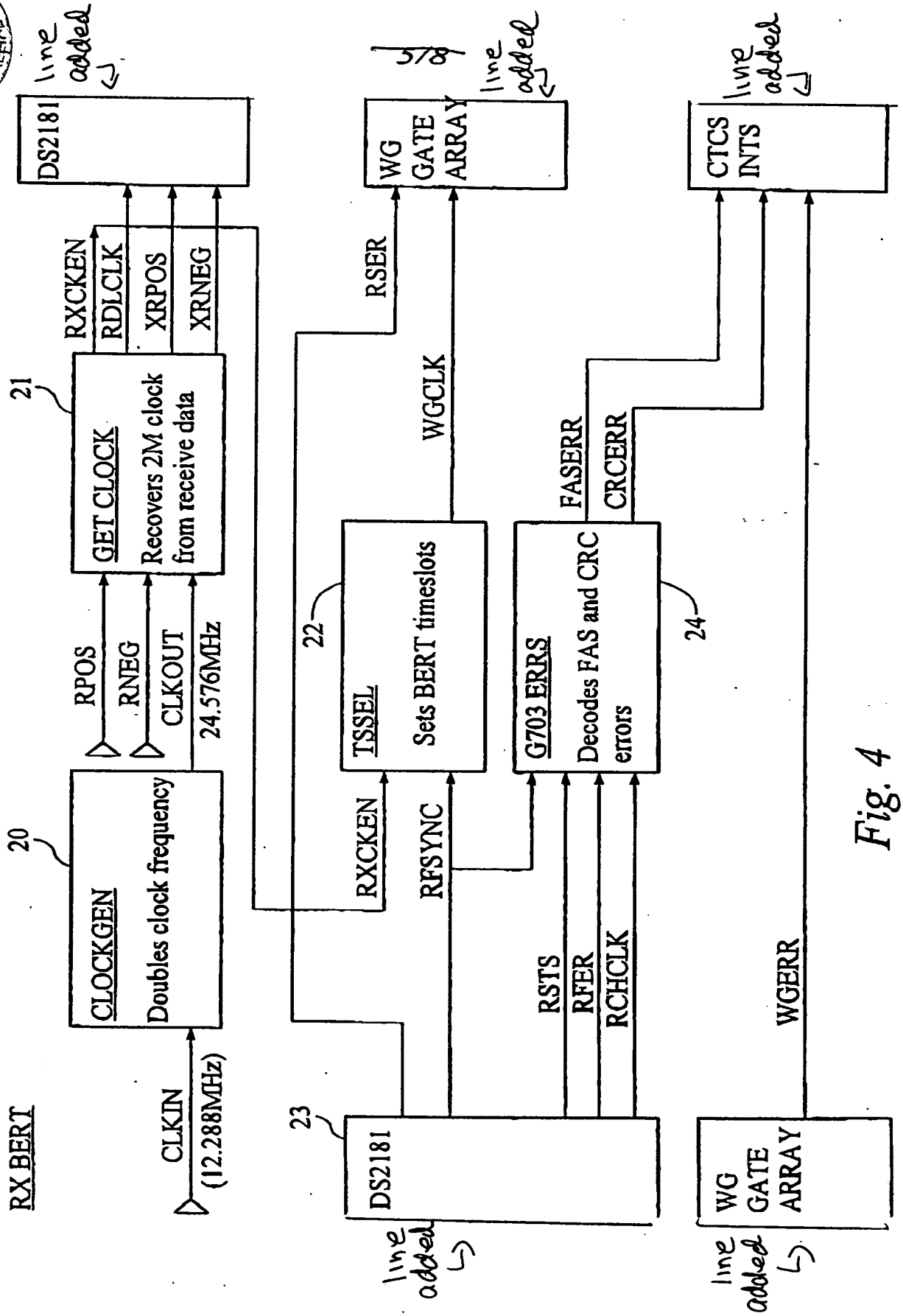


Fig. 4

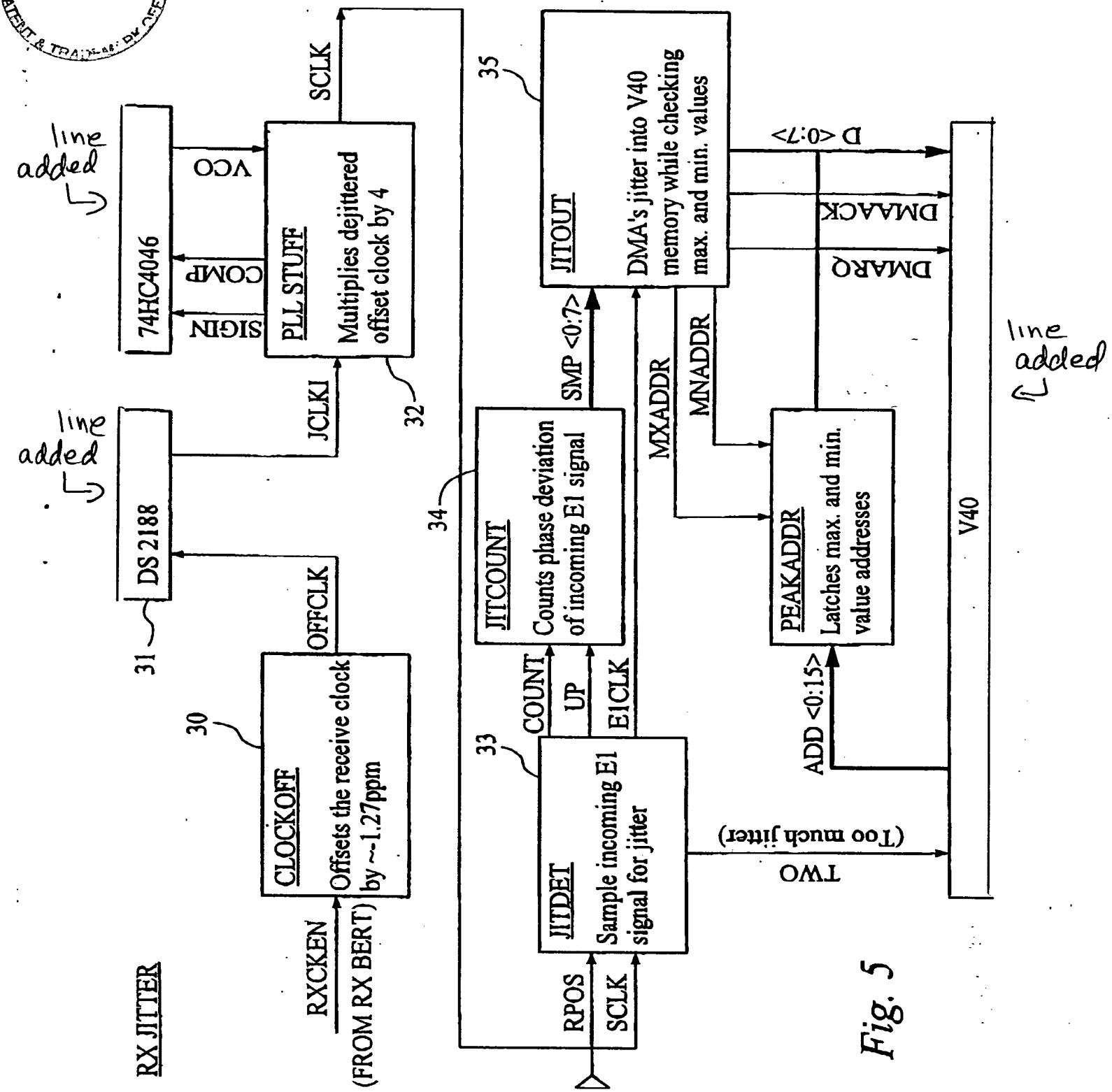


Fig. 5

Application No.: 09/674,444
Amendment Dated October 15, 2004
Reply to Office Action of August 4, 2004
Annotated Sheet Showing Changes

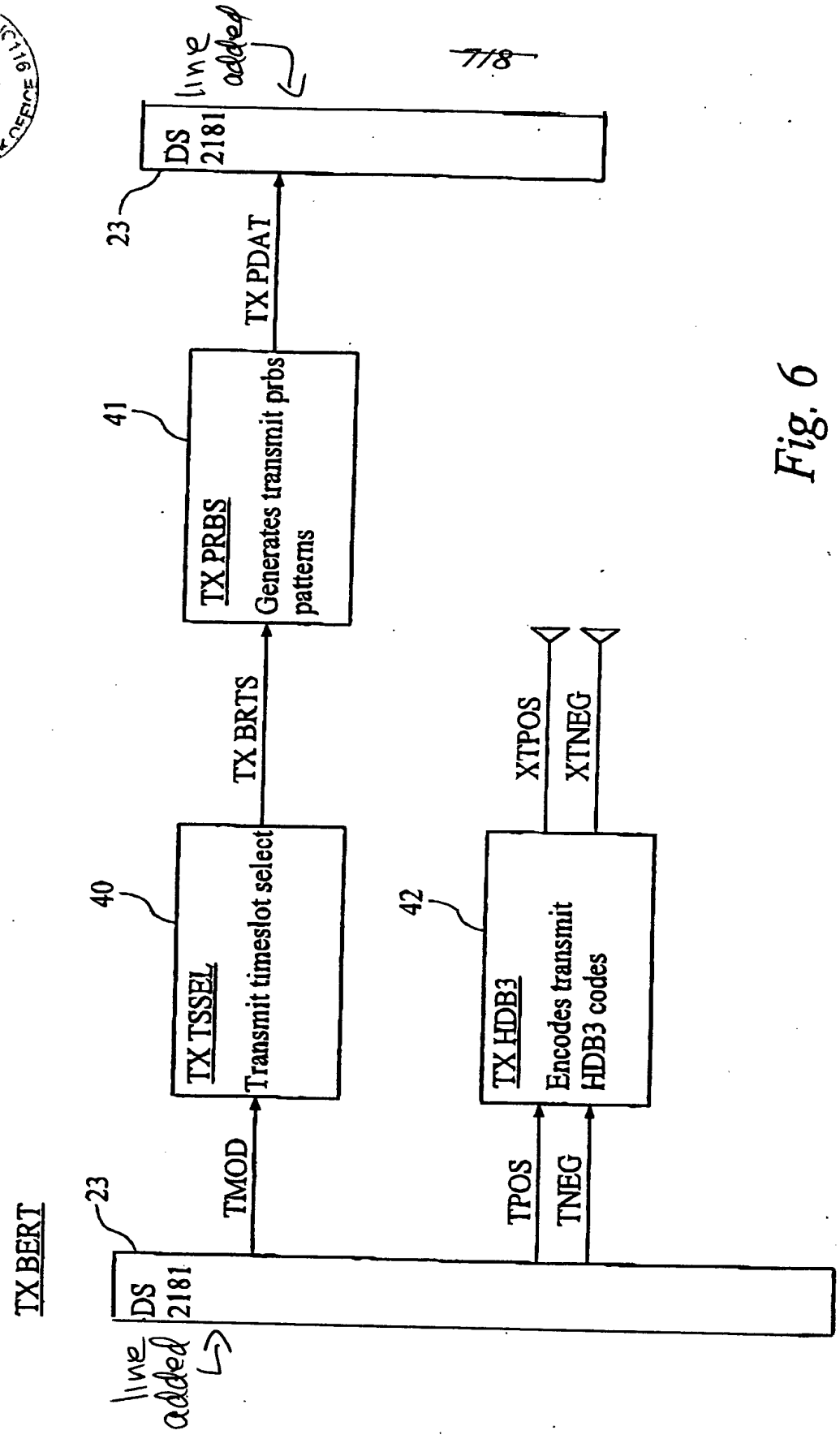


Fig. 6

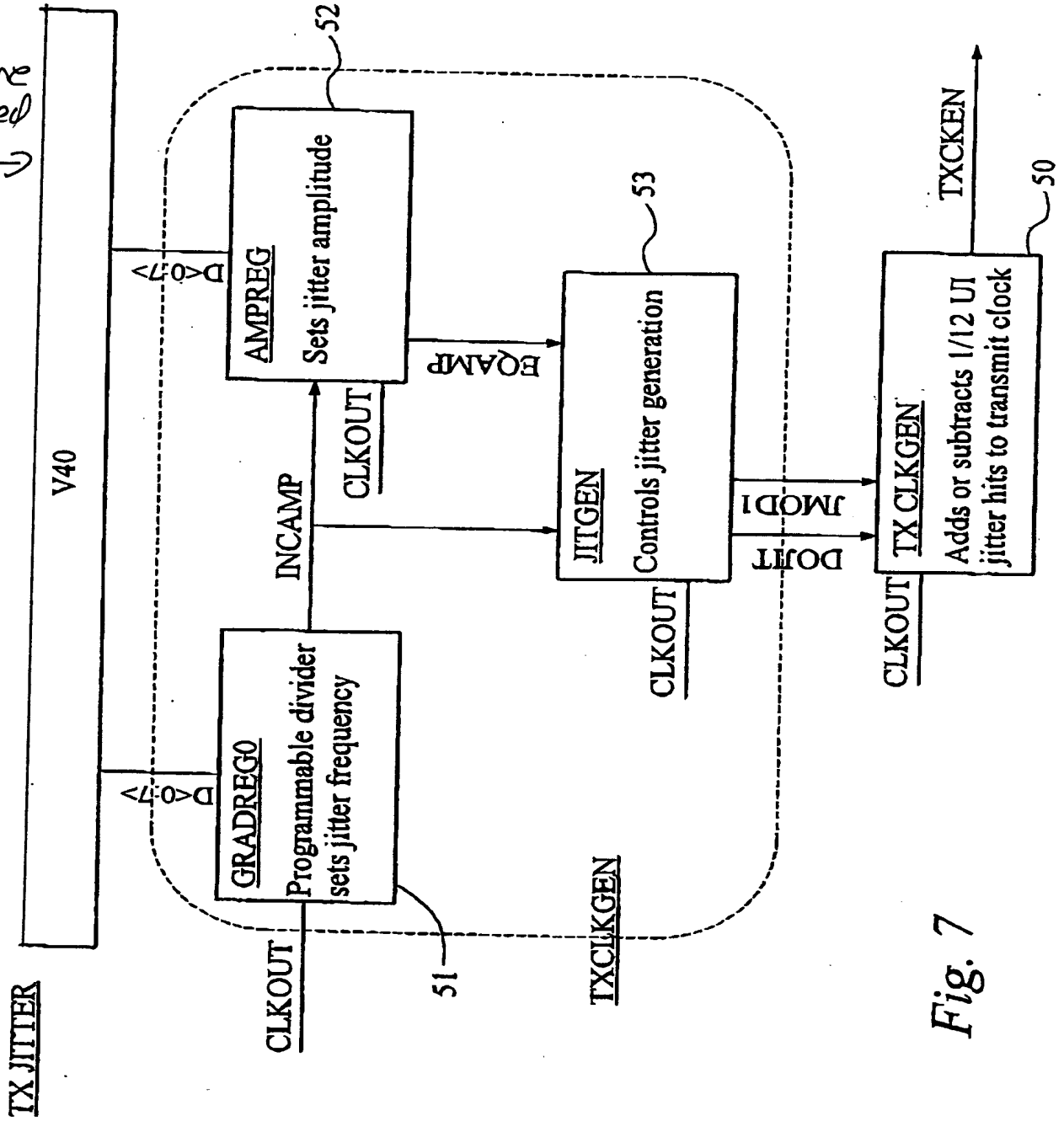


Fig. 7